



# Government Engineering College, Vaishali

**Shyampur, Mansurpur, Bidupur, Vaishali-844115**

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Letter No.: GECV/Office/2026/ 158

Date: 14/02/2026

## NOTICE

The Department of Electronics and Communication Engineering is organizing a **One Week Workshop on "Verilog for Beginners: A Gateway to Semiconductor Industry"** for all interested students. The workshop is designed to provide participants with practical knowledge of **Digital system design using Verilog Hardware Description Language (HDL)**, which forms the foundation of modern VLSI and semiconductor design.

- Date: 16/02/2026 to 22/02/2026
- Time: 2:30 PM to 5:00 PM
- Mode: Offline
- Venue: Seminar hall (3rd Floor)
- Pre-requisite: Basic knowledge of Digital Circuits

The session will cover Verilog fundamentals and hands-on practice with simulators.

Interested students are requested to register their names with given details:

Link: <https://forms.gle/GvrqnrG5tGgKaJu56>

Convener	Mrs. Priyanka Jha (Asst. Professor, ECE department)
Coordinators	Mrs. Neha Choudhary (Asst. Professor, ECE department) Mrs. Perna (Asst. Professor, ECE department)
Expert Session	Mr. Rahul Ranjan (Senior RTL Design Engineer, Qualcomm- Ireland)
Head of Department	Dr. Ravi Ranjan (Asst. Professor, ECE department)
Session Coordinators	Mr. Irfanul Haque (Asst. Professor, ECE department) Mrs. Nivedita Singh (Asst. Professor, ECE department) Mr. Kumar Vimal (Asst. Professor, ECE department) Dr. Tripta (Asst. Professor, ECE department) Mrs. Sunaina Kumari (Asst. Professor, ECE department)

Note: All participating students must ensure minimum 95% attendance for attending the exit exam and get certification.

Refer Appendix I and II for budget estimation and session plan.

Principal

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Copy to:

1. Office, GEC Vaishali
2. Workshop Coordinator, GEC Vaishali
3. Website I/C, GEC Vaishali
4. Office Notice Board, GEC Vaishali

Principal

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